



## 1-OF-10 DECODER

The HEF4028B is a 4-bit BCD to 1-of-10 active HIGH decoder. A 1-2-4-8 BCD code applied to inputs  $A_0$  to  $A_3$  causes the selected output to be HIGH, the other nine will be LOW. If desired, the device may be used as a 1-of-8 decoder with enable; 3-bit octal inputs are applied to inputs  $A_0$ ,  $A_1$  and  $A_2$  selecting an output  $O_0$  to  $O_7$ . Input  $A_3$  then becomes an active LOW enable, forcing the selected output LOW when  $A_3$  is HIGH. The HEF4028B may also be used as an 8-output ( $O_0$  to  $O_7$ ) demultiplexer with  $A_0$  to  $A_2$  as address inputs and  $A_3$  as an active LOW data input. The outputs are fully buffered for best performance.

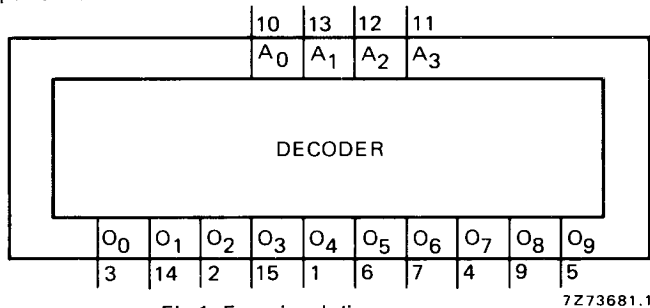


Fig.1 Functional diagram.

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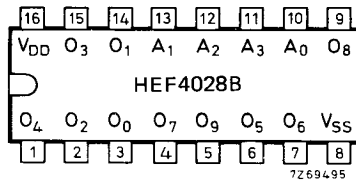


Fig.2 Pinning diagram

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HEF4028BP : 16-lead DIL; plastic (SOT-38Z).  
 HEF4028BD : 16-lead DIL; ceramic (cerdip) (SOT-74).  
 HEF4028BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

### PINNING

$A_0$  to  $A_3$  address inputs, 1-2-4-8 BCD  
 $O_0$  to  $O_9$  outputs (active HIGH)

### FAMILY DATA

$I_{DD}$  LIMITS category MSI

} see Family Specifications

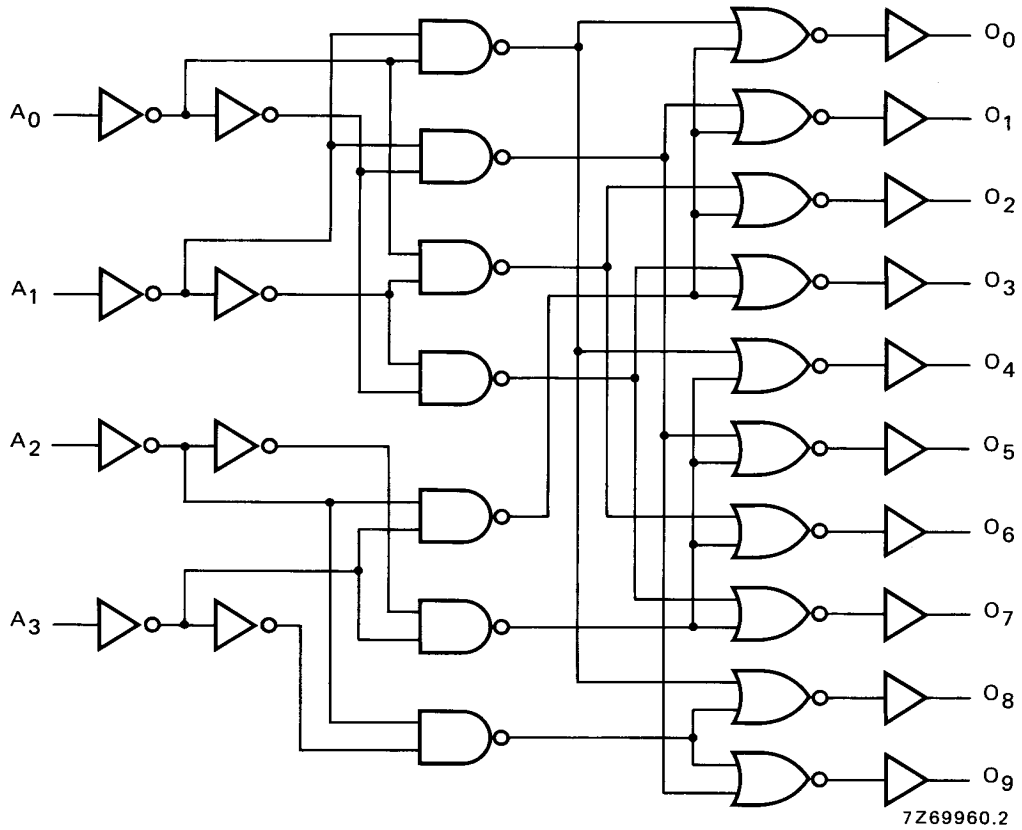


Fig. 3 Logic diagram.

TRUTH TABLE

inputs				outputs										
A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	O <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>	O <sub>9</sub>	
L	L	L	L	H	L	L	L	L	L	L	L	L	L	
L	L	L	H	L	H	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	H	L	L	L	L	L	L	H	L	L	L	L	L	
L	H	L	H	L	L	L	L	L	H	L	L	L	L	
L	H	H	L	L	L	L	L	L	L	H	L	L	L	
L	H	H	H	L	L	L	L	L	L	L	H	L	L	
H	L	L	L	L	L	L	L	L	L	L	L	H	L	
H	L	L	H	L	L	L	L	L	L	L	L	L	H	
H	L	H	L	L	L	L	L	L	L	L	L	L	L	
H	L	H	H	L	L	L	L	L	L	L	L	L	L	
H	H	L	L	L	L	L	L	L	L	L	L	L	L	
H	H	L	H	L	L	L	L	L	L	L	L	L	L	
H	H	H	L	L	L	L	L	L	L	L	L	L	L	
H	H	H	H	L	L	L	L	L	L	L	L	L	L	
				L	L	L	L	L	L	L	L	L	L	L
				L	L	L	L	L	L	L	L	L	L	L
				L	L	L	L	L	L	L	L	L	L	L
				L	L	L	L	L	L	L	L	L	L	L
				L	L	L	L	L	L	L	L	L	L	L
				L	L	L	L	L	L	L	L	L	L	L

H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)

\* Extraordinary states.

## A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}; C_L = 50 \text{ pF}; \text{input transition times} \leq 20 \text{ ns}$ 

	$V_{DD}$ V	symbol	typ.	max.		typical extrapolation formula
Propagation delays $A_n \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	100	200	ns	$73 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		40	80	ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		30	60	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{PLH}$	90	180	ns	$63 \text{ ns} + (0,55 \text{ ns/pF}) C_L$
	10		40	80	ns	$29 \text{ ns} + (0,23 \text{ ns/pF}) C_L$
	15		30	60	ns	$22 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5	$t_{TLH}$	60	120	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$
	10		30	60	ns	$9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$
	15		20	40	ns	$6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$

	$V_{DD}$ V	typical formula for P ( $\mu\text{W}$ )	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
Dynamic power dissipation per package (P)	5	$350 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$2200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$7350 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	